

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of: Doo Yeol RYOO

Serial No.: New Application Group Art Unit: Not Yet Assigned

Filed: July 9, 2003 Examiner: Not Yet Assigned

Title: TRANSISTOR IN SEMICONDUCTOR DEVICES AND METHOD OF FABRICATING THE SAME

**INFORMATION DISCLOSURE STATEMENT**

Honorable Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

July 9, 2003

Sir:

As a means of complying with the duty of disclosure under 37 CFR §1.56, and in accordance with 37 CFR §§1.97 and 1.98, Applicant(s), through the undersigned attorney, submits this Information Disclosure Statement. The patents, publications or other information submitted herewith are listed on the attached Form PTO-1449 and copies are attached.

In accordance with 37 CFR §1.97(b)(1) or (2), this Information Disclosure Statement is being filed either within three months of the filing date of the above-identified application, or within three months of the date of entry into the national stage of the above-identified application as set forth in 37 CFR §1.491. Accordingly, no fee is required.

Respectfully submitted,

JACOBSON HOLMAN, PLLC

By: *Harvey B. S. Ham Jr.* RN 20,851  
Yoon S. Ham  
Registration No. 45,307

400 Seventh Street, N.W.  
Washington, DC 20004  
(202) 638-6666

Atty. Dkt. No.: P68972US0  
YSH:kyc

JACOBSON HOLMAN, PLLC  
400 SEVENTH STREET, N.W.  
WASHINGTON, D.C. 20004-2201

## LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.: P68972US0 GROUP ART UNIT: Not Yet Assigned  
SERIAL NO.: New Application FILING DATE: July 9, 2003  
APPLICANT(S): Doo Yeol RYOO TODAY'S DATE: July 9, 2003

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U.S. PATENT DOCUMENTS

*EXAMINER <u>INITIAL</u>	DOCUMENT NUMBER	DATE	NAME	INT'L CLASS	SUB- CLASS	FILING DATE (If Appropriate)
AA	_____	_____	_____	_____	_____	_____
AB	_____	_____	_____	_____	_____	_____

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FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	SUB- CLASS	TRANSLATION (YES) (NO)
AC	_____	_____	_____	_____	_____
AD	_____	_____	_____	_____	_____

\*\*\*\*\*  
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AE	<u>C.H.Chen, et al; "Thermally-Enhanced Remote Plasma Nitrided Ultrathin (1.65nm) Gate Oxide with Excellent Performances in Reduction of Leakage Current and Boron Diffusion"; IEEE Electron Device Letters, Vol.22, No. 8; August 2001; pp.378-380.</u>
AF	<u>Hoon Lim, et al; "The Effects of STI Process Parameters on the Integrity of Dual Gate Oxides"; IEEE 01CH37167 39th Annual International Reliability Physics Symposium, 2001; pp. 48-51.</u>
AG	<u>S.Song, et al; "On the Gate Oxide Scaling of High Performance CMOS Transistors"; 2001 IEEE; IEDM 01-55 to IEDM 01-58.</u>

EXAMINER	DATE CONSIDERED
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\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).